each of the second charge circuit and the second bias circuit includes a PMOS transistor.

20. A driver circuit configured to charge a conductive line connected to a plurality of memory cells of a nonvolatile memory, the driver circuit comprising:

a clamp switch including a gate configured to receive a clamp voltage, a first node, and a second node connected to a charge node of the conductive line;

a charge circuit connected to the first node of the clamp switch,

the charge circuit being at least one of configured to drain a current from the charge node through the clamp switch and configured to supply a current to the charge node through the clamp switch;

a comparison voltage generator configured to output a comparison voltage;

a single stage amplifier,

the single stage amplifier being configured to amplify a difference between the comparison voltage and a voltage of the charge node, and

the single stage amplifier being configured to output the clamp voltage as the amplification result; and

a current bias circuit connected to the gate of the clamp switch,

the current bias circuit being configured to adjust the amount of current flowing to a ground node to which a ground voltage is supplied through the comparison voltage generator, the single stage amplifier, and the current bias circuit.

21.-**25**. (canceled)

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